## REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5-20 are presently pending in this application, Claims 5-18 having been withdrawn from further consideration by the Examiner, Claim 4 having been canceled, Claims 1-3 and 19 having been amended and Claim 20 having been added by the present amendment.

In the outstanding Office Action, Claims 1, 4 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Strandberg et al. (U.S. Patent 6,323,435) in view of Tsukada et al. (U.S. Patent 6,809,415); and Claims 2 and 3 were rejected under 35 U.S.C. §103(a) as being unpatentable over the modified board of Strandberg et al. in view of Westbrook et al. (U.S. Patent 6,203,967).

Claims 1-3 and 19 have been amended and Claim 20 has been newly added herein. These amendments and addition in the claims are believed to find support in the specification, claims and/or drawings as originally filed, for example, the specification, page 19, line 12, to page 20, line 6, and page 21, lines 5-12, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the rejection based on the cited reference, a brief review of Claim 1 as currently amended is believed to be helpful. Claim 1 is directed to a multilayer printed wiring board and recites: "a core substrate having a first surface and a second surface on an opposite side of the first surface; a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively, and comprising one of a power source conductor and a grounding conductor; a plurality of interlayer insulation layers formed

on the first conductive layers, respectively, and the core substrate; and a plurality of second conductive layers formed on the interlayer insulation layers, respectively, wherein the first conductive layers on the core substrate have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers, and each of the first conductive layers on the core substrate has a side face which is tapered such that an angle, $\Theta$, formed by a straight line connecting the top end and bottom end of the side face of each of the first conductive layers and a horizontal face of the core substrate satisfies $2.8 < \tan \Theta < 55$."

By providing such a power source conductor, a loop inductance of a power supply, the core substrate and an electronic component can be decreased, and power shortage in an initial operation is decreased to reduce the possibility of power shortage, allowing an electronic component such as an IC chip with a high frequency range can be mounted on the printed wiring board of Claim 1 without occurrences of malfunction and/or error in the initial operation. Also, by providing such a grounding conductor, noises do not superimpose on the signal of an IC chip and the supply of power to the chip, thereby preventing malfunction and/or error.

It is respectfully submitted that Strandberg et al. does not teach or suggest "a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively, and comprising one of a power source conductor and a grounding conductor ..., wherein the first conductive layers on the core substrate have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers ..." as recited in amended Claim 1.

On the other hand, Strandberg et al. simply states that the conductive traces 14a , 14 b in Figs. 1-5 typically have a thickness in the range of 20 $\mu$m to 30 $\mu$m[1] and that the wiring pattern on the substrate 112 has a thickness in the range of 10 $\mu$m to 20 $\mu$m.[2] According to Strandberg, it is believed that the conductive pattern on the surface 112a of the substrate 112 should be made much thinner with much less filler to provide a lower dielectric constant to the structure and thus a lower impedance.[3] As such, it is believed that Strandberg teaches away from the conductive layers on the core substrate having a thickness which is larger than a thickness of the conductive layers on the interlayer insulation layer. Therefore, the structure recited in Claim 1 is clearly distinguishable from Strandberg.

Tsukada et al. merely describes providing superior adhesion between a substrate and a conductor pattern by forming a conductor pattern with a trapezoidal cross-section and a solder resist coated on the conductor pattern, and Westbrook et al. describes providing a grounding plane layer (a patterned conductive layer or a metal clad conductive layer) on the surface of a high density interconnect wiring board, *not a core substrate*. Thus, Tsukada et al. and Westbrook et al. are not believed to teach or suggest the first conductive layers as recited in amended Claim 1, and the structure recited in Claim 1 is also believed to be distinguishable from Tsukada et al. and Westbrook et al.

Because none of Strandberg et al., Tsukada et al. and Westbrook et al. discloses the conductive layers as recited in Claim 1, their teachings even in combination are not believed to render the structure recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2, 3, 19 and 20 depend from Claim 1, substantially the same arguments set forth

[1] See Strandberg, column 8, lines 4-9.
[2] See id., column 9, lines 16-23.
[3] See Strandberg, column 9, lines 23-34.

above also apply to these dependent claims. Hence, Claims 2, 3, 19 and 20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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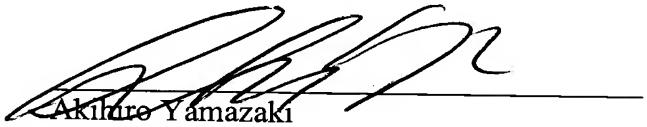

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